

TIMING CHARACTERISTICS

$AV_{DD} = V_{BOOST_X} = 15\text{ V}$; $AV_{SS} = -15\text{ V}$; $DV_{DD} = 2.7\text{ V to }5.5\text{ V}$; $AV_{CC} = 4.5\text{ V to }5.5\text{ V}$; dc-to-dc converter disabled; $AGND = DGND = GND_{SW_X} = 0\text{ V}$; $REFIN = 5\text{ V}$; voltage outputs: $R_L = 1\text{ k}\Omega$, $C_L = 220\text{ pF}$; current outputs: $R_L = 300\ \Omega$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter ^{1, 2, 3}	Limit at T_{MIN} , T_{MAX}	Unit	Description
t_1	50	ns min	SCLK cycle time
t_2	17	ns min	SCLK high time
t_3	17	ns min	SCLK low time
t_4	20	ns min	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time
t_5	15	ns min	24 th /32 nd SCLK falling edge to $\overline{\text{SYNC}}$ rising edge (see Figure 79)
t_6	500	ns min	SYNC high time following a configuration write
	5	$\mu\text{s min}$	SYNC high time following a DAC update write
	20	$\mu\text{s min}$	SYNC high time following a DAC update write (slew rate control enabled)
t_7	15	ns min	Data setup time
t_8	10	ns min	Data hold time
t_9	20	$\mu\text{s min}$	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge (applies to any channel with digital slew rate control enabled; single DAC updated)
	5	$\mu\text{s min}$	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge (applies to any channel with digital slew rate control disabled; single DAC updated)
t_{10}	10	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{11}	520	ns max	$\overline{\text{LDAC}}$ falling edge to DAC output response time
t_{12}	See the AC Performance Characteristics section	$\mu\text{s max}$	DAC output settling time
t_{13}	5	$\mu\text{s min}$	CLEAR high time
t_{14}	9	$\mu\text{s max}$	CLEAR activation time
t_{15}	45	ns max	SCLK rising edge to SDO valid
t_{16}	5	$\mu\text{s min}$	$\overline{\text{SYNC}}$ rising edge to DAC output response time ($\overline{\text{LDAC}} = 0$) (single DAC updated)
t_{17}	500	ns min	$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ rising edge
t_{18}	1	$\mu\text{s min}$	$\overline{\text{RESET}}$ pulse width

¹ Guaranteed by design and characterization; not production tested.

² All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.

³ See Figure 3, Figure 4, Figure 6, and Figure 7.

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³ See Figure 3, Figure 4, Figure 6, and Figure 7.